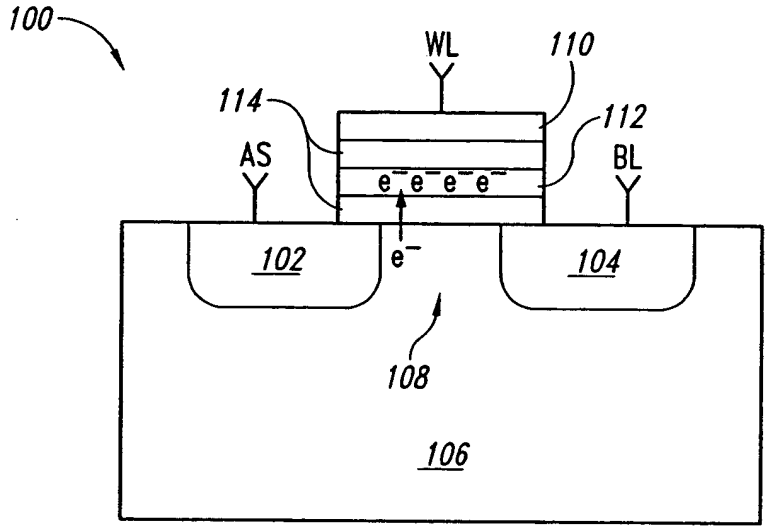

Fig. 1
(Background Art)

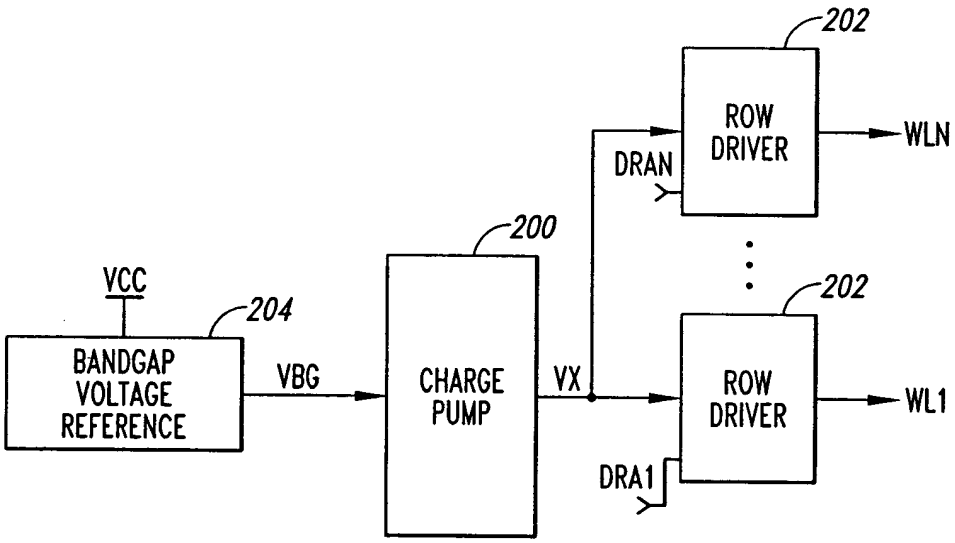

Fig. 2
(Background Art)

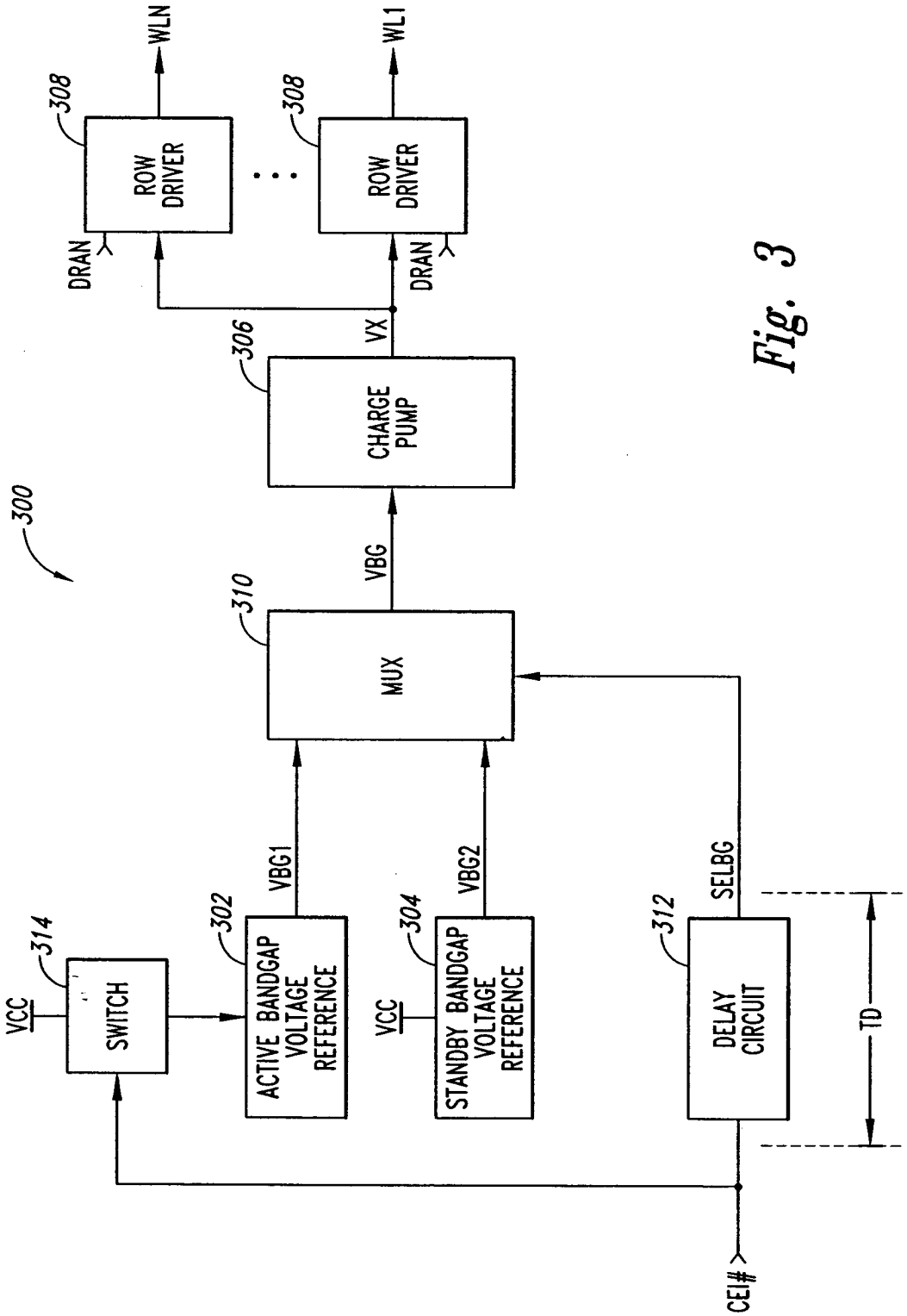
300
308
ROW DRIVER
WLN
WL1
DRAN
306
CHARGE PUMP
VX
VBG
310
MUX
VBG1
VBG2
SELBG
302
ACTIVE BANDGAP VOLTAGE REFERENCE
304
STANDBY BANDGAP VOLTAGE REFERENCE
312
DELAY CIRCUIT
TD
314
SWITCH
VCC
CE#

Fig. 3

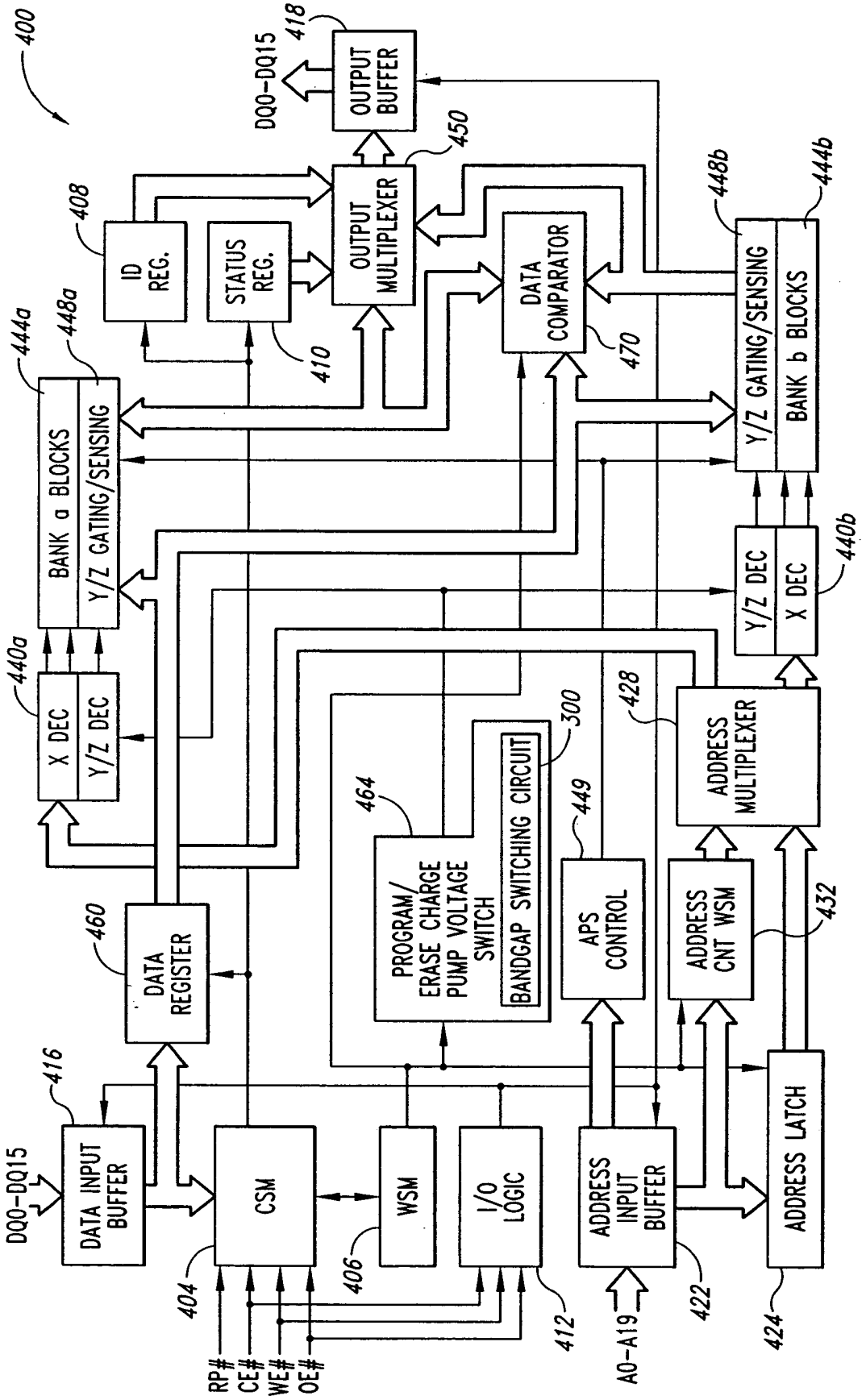
400
DQ0–DQ15
418
OUTPUT BUFFER
450
OUTPUT MULTIPLEXER
408
ID REG.
STATUS REG.
410
DATA COMPARATOR
470
448a
444a
BANK a BLOCKS
Y/Z GATING/SENSING
448b
444b
Y/Z GATING/SENSING
BANK b BLOCKS
440a
X DEC
Y/Z DEC
440b
Y/Z DEC
X DEC
428
ADDRESS MULTIPLEXER
464
PROGRAM/ ERASE CHARGE PUMP VOLTAGE SWITCH
BANDGAP SWITCHING CIRCUIT
300
449
APS CONTROL
ADDRESS CNT WSM
432
460
DATA REGISTER
416
DQ0–DQ15
DATA INPUT BUFFER
CSM
WSM
I/O LOGIC
ADDRESS INPUT BUFFER
ADDRESS LATCH
404
406
412
422
424
A0–A19
RP#
CE#
WE#
OE#

Fig. 4

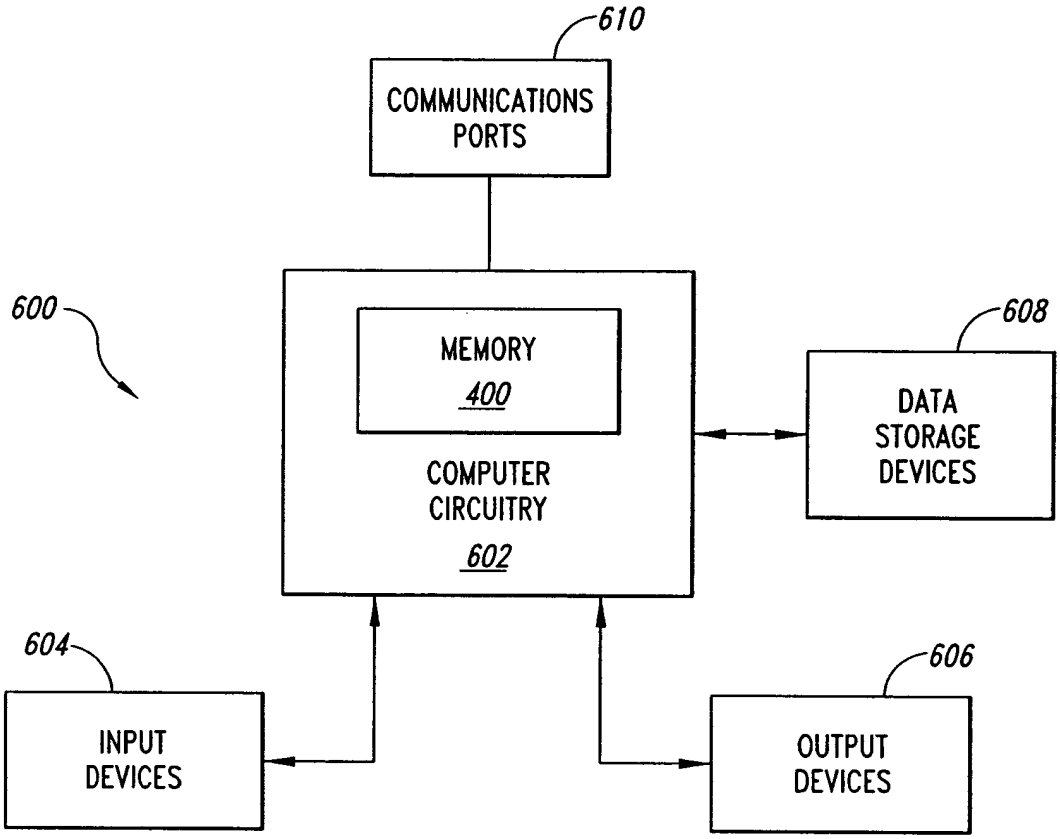
610
COMMUNICATIONS PORTS
600
MEMORY
400
COMPUTER CIRCUITRY
602
608
DATA STORAGE DEVICES
604
INPUT DEVICES
606
OUTPUT DEVICES

Fig. 5